ABSTRACT OF THE DISCLOSURE

A counter counts pulses of a clock generated by an oscillator. A control register clears the counted value, in response to a reset signal sent from an external circuit. In the case where the counted value exceeds a limit value, an output control circuit outputs a

5 reset signal for instructing to execute the reset process, to the external circuit. This reset signal is provided also to the control register. The control register controls the counter to count the pulses of the clock, in response to the reset signal. Then, abnormal operations occurring in the external circuit during the execution of the reset process can be detected.